Remarks:

Reconsideration of the application, as amended herein is respectfully requested.

Claims 8 - 10 are presently pending in the application. New claims 9 and 10 have been added. As it is believed that claim 8 was patentable over the cited art in its original form, that claim has not been amended to overcome the reference.

In item 5 of the above-identified Office Action, claim 8 was rejected as allegedly being indefinite under 35 U.S.C. § 112, first paragraph. Similarly, in item 7 of the Office Action, claim 8 was rejected as allegedly also being indefinite under 35 U.S.C. § 112, second paragraph. Both 35 U.S.C. § 112 rejections stem from an allegation in the Office Action, that the claim did not specify whether the adding unit and the subtracting units **were separate units** or **a combined unit.** More particularly, although the Office Action acknowledged that the specification of the instant application supported having an adder and subtractor in a **combined** unit, the Office Action alleged that Applicants' specification did not support the adding and subtracting unit being separate units, and thus claim 8 was indefinite under 35 U.S.C. § 112, first and second paragraphs. Applicants respectfully disagree.

More particularly, Applicants' claim 8 is supported by the specification of the instant application. For example, the specification of the instant application recites that the instruction length may be **added or subtracted** from another value, to produce the relative address computation. for example, page 11 of the instant application, lines 13 - 16, state:

> **According to a fourth embodiment of the invention**, the value of the instruction length may also **be added** to an offset value which is used for the computation of the relative addresses, **or may be subtracted** from the offset value. [emphasis added by Applicants]

See also, page 5 of the instant application, line 18 - page 6, line 4, states:

> Similarly, it is preferably possible according to the invention, **dependent on the various operating states or assembler codes, to add or subtract the instruction length to or from the program counter reading for the relative address computation**, or to leave the program counter reading unchanged.
>
> **Similarly, it is possible according to the invention, dependent on the various operating states or assembler codes, to add, or subtract, an instruction length to or from the offset value**, which is usually used for the computation of relative addresses, or to leave the offset value unchanged in each case. [emphasis added by Applicants]

Applicants note that, under common Boolean mathematics, as well as, in terms of speech and language, the statement "a or b" includes the possibilities of: 1) just a; 2) just b; and 3) the combination of **a and b**. As such, the disclosure in the

specification of adding **or** subtracting, additionally supports Applicants' claim 8, reciting **both** an adding unit **and** a subtracting unit.

Additionally, page 12 of the instant application, lines 13 - 25, describes **the operation of a fourth embodiment of the instant invention incorporating both adding and subtracting units**, stating:

> According to the invention, for example, when using the address of the current instruction line in the instruction counter of the microprocessor, **the instruction length can then optionally be added to the offset value** if using an assembler that specifies that the instruction counter must point to the next assembler instruction.
>
> Similarly, **when managing the address of the next assembler instruction** in the instruction counter of the processor, **the instruction length can be subtracted from the offset value** if an assembler for which the instruction counter must always point to the current assembler instruction is to be processed. [emphasis added by Applicants]

As such, Applicants' specification describes at least one embodiment of the invention **wherein a first instruction can be addressed by adding the instruction length to an offset value, while the very next instruction can be differently relatively addressed by subtracting the instruction length from the offset value.** One particular advantage to the invention of claim 8 (i.e., integrating both an adder and a subtractor) is

that it is possible to switch between different program counter and assembler codes, faster.

Further, that the adding unit and subtracting unit **can be separate** is also supported by the specification of the instant application. For example, Figs. 2 and 3 of the instant application, as originally filed, show a **separate** adder (Fig. 2) and a **separate** subtractor (Fig. 3), located between the counter and the computation unit. In view of the specification (i.e., " . . . it is preferably possible according to the invention, **dependent on the various operating states or assembler codes, to add or subtract** the instruction length to or from the program counter reading for the relative address computation"), the illustration in Figs. 2 and 3 of the instant application supports that that the units could, **additionally**, be separate units. As such, Applicants' believe that claim 8, reciting **both** an adder and a subtractor (whether separate **or combined**), is supported by the specification of the instant application, as filed. As such, Applicants' claim 8 is believed to comply with the written description requirement of 35 U.S.C. § 112, first paragraph, as well as the definiteness requirement of 35 U.S.C. § 112, second paragraph.

Additionally, Applicants' new claim 9 recites, among other limitations:

> **an adding unit connected between said program counter and said computation unit**, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; **or**
>
> **a subtracting unit connected between said program counter and said computation unit for the relative addresses**, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit. [emphasis added by Applicants]

As such, Applicants' invention of claim 9 recites, among other limitations, an **adding unit or a subtracting unit**, connected between the program counter and the computation unit for the relative addresses. Applicants' new claim 9 is supported by the specification of the instant application, for example, page 11 of the instant application, lines 13 - 16; page 5 of the instant application, line 18 - page 6, line 4; and the figures of the instant application.

Further, Applicants' new claim 10 recites, among other limitations:

> an adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit;

a subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; and

said adding unit and said subtracting unit being a combined unit. [emphasis added by Applicants]

Items 5 and 7 of the Office Action acknowledge the support in the specification of the instant application for an adding unit and subtracting unit being in a combined unit, as presently recited by new claim 10.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first / second paragraphs.

In item 9 of the above-identified Office Action, claim 8 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,854,913 to Goetz et al ("**GOETZ**"), in view of U. S. Patent No. 5,088,030 to Yoshida ("**YOSHIDA**") [sic], May et al., "The PowerPC Architecture", 1994 ("**POWERPC**") and K. Short, "Embedded Microprocessor Systems Design", 1998 ("**SYSTEMS DESIGN**") and in view of U. S. Patent No. 5,983,018 to Kanzaki ("**KANZAKI**").

Applicants respectfully traverse the above rejections.

More particularly, all of Applicants' claims require, among other limitations, **an adding unit and/or a subtracting unit, each having a third input for receiving a parameter.**

Page 9 of the Office Action states, in part:

> Goetz, Yoshida, and May failed to teach an addition unit having a third input receiving parameter, and a subtracting unit having a third input receiving parameter.

Rather, the Office Action pointed to **KANAZAKI** as allegedly disclosing the above elements missing from **GOETZ**, **YOSHIDA** and **MAY**. Applicants respectfully disagree.

More particularly, the **KANZAKI** reference discloses a microcomputer for checking a flag in a flag circuit to determine whether or not to **decrement the count of a program counter**. In contrast to Applicants' claims, **KANZAKI** does not teach Applicants' particularly claimed addition unit or subtraction unit (i.e., including an input from a multiplexer, etc.), as claimed by Applicants. Further, there is no teaching, suggestion or motivation in **KANZAKI** or **YOSHIDA** to combine those references in the manner suggested in the Office Action. For example, The Office Action alleged that a flag from **KANZAKI** would provide indicate an exception to the adder 15 of Fig. 2 of **YOSHIDA**. However, the references do not

provide any teaching, suggestion or motivation to do so, nor would such motivation be apparent to a person of ordinary skill in the art from the general knowledge in the art. As stated on page 10 of the Office Action, **YOSHIDA** fails to teach interrupt and exception handling.

Further, the combination of references made in the Office Action still does not teach or suggest all limitations of Applicants' claims. **KANZAKI** discloses **decrementing the program counter by a predetermined amount,** in responsethe closing of the switch 44. This can be seen from col. 6 of **KANZAKI**, lines 31 - 48, cited in the Office Action, and which state:

> FIG. 6 is a block diagram of an address generating circuit in the microcomputer furnished as the second embodiment of the invention. In FIG. 6, reference numeral 40 is a program counter that accommodates an address in the program memory 15 of the next instruction to be executed by the CPU 10; 41 is an adder that adds "1" to the contents of the program counter 40 (i.e., program counter value); **42 is a subtractor that subtracts a predetermined value such as "2" from the contents of the program counter 40;** 43 is a switch turned on or off every time the CPU 10 executes an instruction in order to increment the contents of the program counter 40; and 44 is a switch turned on or off by the flag that is outputted onto the flag output line 35. **When the flag is found to be set, the switch 44 causes the subtractor to subtract a predetermined value from the contents of the program counter 40.** A suitable portion of the usually furnished hardware of the microcomputer 1 doubles as the address generating circuit.

As such, **KANZAKI** produces a flag to **subtract a preset value from the program counter**. If combinable with **YOSHIDA**, arguendo, as set forth in the Office Action, the combination of **KANZAKI** and **YOSHIDA** would cause a preset (i.e., predetermined) value to be decremented from the program counter of **YOSHIDA**. This is not the same as the subtraction unit claimed by Applicants, which requires, among other things, having a first input connected to the program counter, **a second input connected to said multiplexer**, a third input receiving the parameter. Applicants' claimed multiplexer requires, among other things, **a first input, a second input for receiving a 0 value**, and a third input receiving a parameter designating a respective assembler code **and, depending on how the parameter is set, a different relative addressing takes place**.

As such, Applicants' **claimed** subtraction unit can provide different results, **based upon the input from the multiplexer**. The subtraction taught by the combination of **KANZAKI** and **YOSHIDA** would always require the **same** result, caused by **KANZAKI**'s teaching of **always decrementing the program counter by the same preset value**, when the flag is found to be set. As such, the combination of references, including **KANZAKI** and **YOSHIDA**, made in the Office Action still fails to teach or suggest, among other limitations of Applicants' claims,

Applicants' particularly claimed adder and/or subtractor receiving an input from the particularly recited multiplexer.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 8 - 10. Claims 8 - 10 are, therefore, believed to be patentable over the art.

In view of the foregoing, reconsideration and allowance of claims 8 - 10 are solicited.

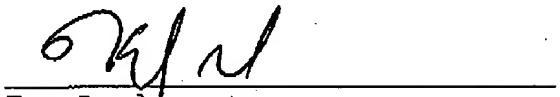
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Applic. No. 09/928,011
Response Dated July 19, 2007
Responsive to Office Action of April 19, 2007

Respectfully submitted,



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